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FLEXIBLE DATA LINK

APRIL 2015

FINAL TECHNICAL REPORT

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14. ABSTRACT The primary objective of this effort was to build a system that can operate in contested environments (the anticipated future combat fields). Operating in contested environments requires flexible waveform characteristics that can change on-the-fly based on conditions of the combat mission. The Flexible Data Link system is designed with the capability of handling data rates up to 25 Bbps. The high speed operation will most likely be utilized in permissive environment operations where we have air dominance. Data rates can be substantially lowered when operating in contested/highly contested environments. In order to overcome atmospheric conditions, the modular design of the Flexible Data Link allows the digital backend to be connected to a variety of analog frontends. Any frontend (RF, FSO, or IR) can be used as long as it follows the specifications of the standard interface to the digital backend.					
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Summary:

The primary objective of this effort is to build a system that can operate in dynamic military environments that require flexible waveform characteristics that can change on-the-fly based on conditions of the mission.

The Flexible Data Link system is designed with the capability of handling data rates up to 25 Gbps. The high speed operation will most likely be utilized in permissive environment operations where we have air dominance. Data rates can be substantially lowered when operating in congested or contested RF environments.

In order to overcome atmospheric conditions, the modular design of the Flexible Data Link allows the digital backend to be connected to a variety of analog frontends. Any frontend (RF, FSO, or IR) can be used as long as it follows the specifications of the standard interface to the digital backend.

Introduction:

This report describes progress made during the period of September 2013 through September 2014 on the in-house Flexible Data Link project. The primary objective of this project is to build a flexible high speed data link that can survive operations in contested as well as permissive environments. To be able to achieve this goal, the communication system is required to have the capability of reconfiguring the waveform characteristics (on-the-fly) based on the engagement environment. Therefore, flexibility was the highest priority in the design of the Flexible Data Link system.

One of the potential operating modes that can survive contested environments is to operate in burst mode. In burst mode, the communication system transmits data in a very high rate for a short period of time. Therefore, the Flexible Data Link system is designed to handle data rates up to 25 Gbps (peak performance). This mode of operation helps conceal the footprint of the transmitter. At the same time, during silent times, the system can be utilized for another mission such as SIGINT to form a multi mission RF system.

During this phase of the effort, the AFRL in-house team completed the preliminary design review (PDR) and the critical design review (CDR) milestones. The S&E community at AFRL as well as people from the academia was invited to the design reviews to exchange ideas and refine our design.

The following sections explain the technical details of the effort performed in the above period. A decision was made to follow this effort with the next phase. Next phase will be used to build the actual hardware.

Methods, Assumptions, and Procedures:

This phase of the effort did not include testing. The primary goal of this phase was to complete the PDR and CDR reviews. Upon the approval of the design, the team will move forward to build the hardware.

The primary method used during the design phase is peer reviews. During the course of this effort, the team held regular technical meetings to exchange ideas and discuss alternatives about the components design of the system.

In addition to team technical discussions, the S&E community at AFRL was invited to attend the presentations of both the PDR and CDR. Feedback from subject matter experts from the S&E community as well as people from the academia were taken into consideration in the design of the system

Results & Discussion:

The following sections detail a discussion and the results of the design phase of the Flexible Data Link system

Flexible Data Link System Characteristics

The Flexible Data Link system consists of the usual communications system components: Forward Error Correction (FEC), Modulation, Equalization, Synchronization, etc. Since it was determined that this system will have Orthogonal Frequency Division Multiplexing (OFDM) as its base data carrier (with various modulation schemes on top of each subcarrier), other processing is involved, namely: Fourier Transformation (FFT and IFFT), Cyclic Prefix (CP) appending, Peak to Average Power (PAPR) mitigation, and parallel processing. Furthermore, the utilization of digital upconversion (DUC) and digital downconversion (DDC) results in more complicated digital (FPGA) processing, yet simplifies the analog design significantly while improving the quality of the transmitted signal. A high-level system block diagram can be found in Figure 1; many of these blocks will be discussed in later sections.

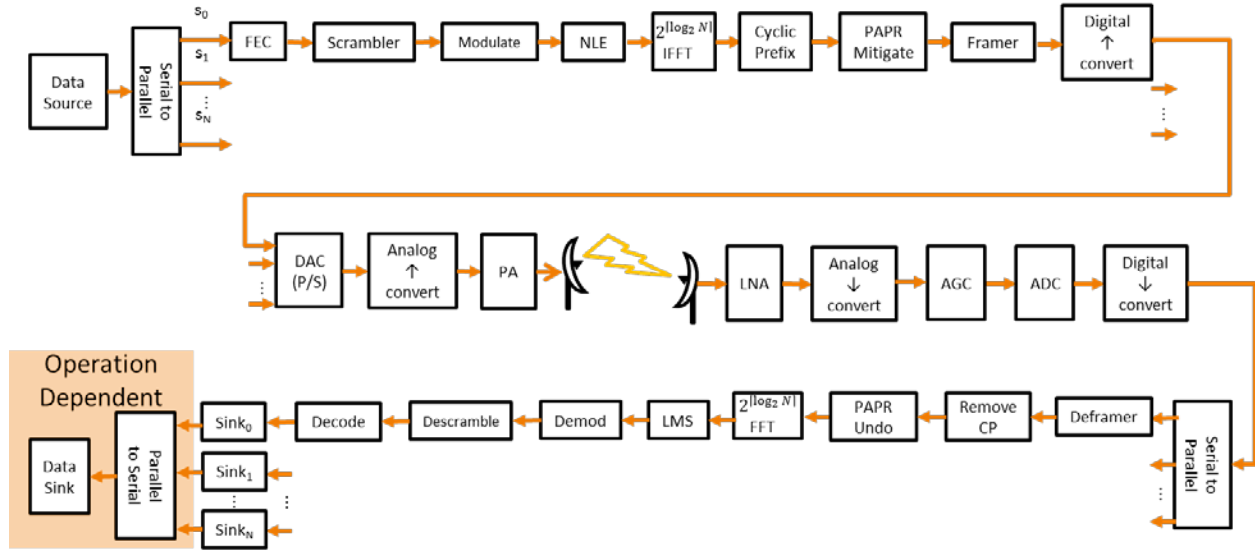


Figure 1: Flexible Data Link System Diagram

Cyclic Prefix Determination

The design of a communications system that relies on OFDM typically begins with selecting the desired multipath tolerance. This is the amount of delay (time) spread we expect from receiving the direct path of the transmitted signal to the last (significant) reflected path of the same transmitted signal. The delay spread is caused by scattering of the signal by natural or man-made objects in between the transmitter and receiver. The selection of this multipath tolerance (known as the CP) is crucial; selecting a duration too small will allow delayed scatters to interfere with neighboring OFDM symbols, whereas overcompensating lowers the throughput of the transmission. The CP is a copy of the end portion of an OFDM symbol added to the beginning. A diagram of the CP is found in Figure 2.

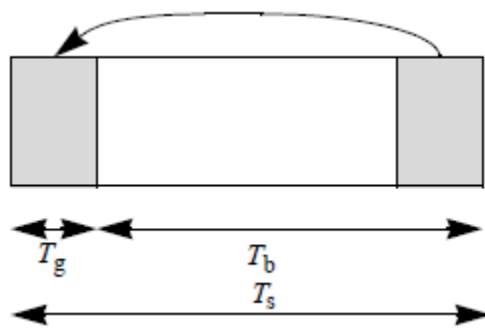


Figure 2: Cyclic Prefix duration of an OFDM symbol

The desired (unique) data transmission duration is T_b , which contains the useful information to convey. The replica duration T_g is added at the beginning of the symbol, creating a duration T_s . The value of T_g is found through the two multipath scenarios. The first is a single reflection from

the aircraft to a ground antenna. Utilizing the threshold system requirements (100 km range), we calculate the multipath of the aircraft as it approaches the ground antenna.

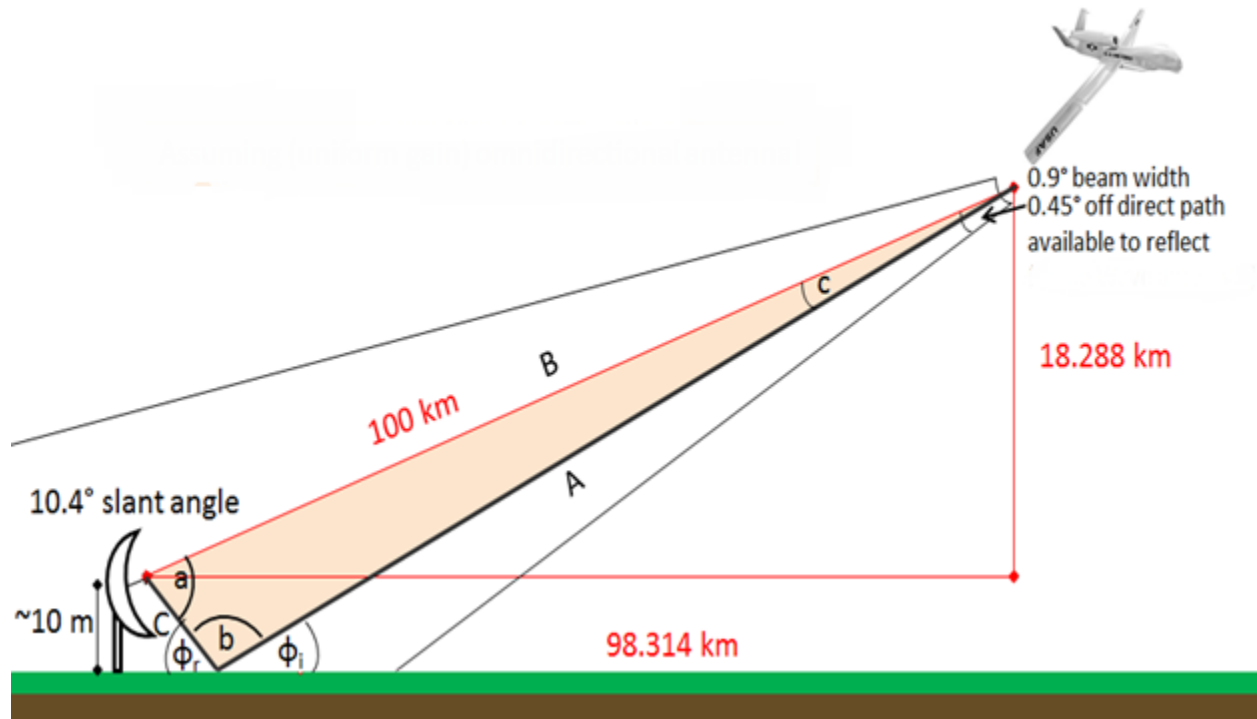


Figure 3: Multipath scenario #1

The calculation of the reflected path (denoted as A + C in Figure 3) is found through the Law of Sines:

$$\phi_i = \phi_r = 10.4113^\circ, B = 100000.0 \text{ m}, a = 10.4 + \phi_i = 20.8113^\circ$$

$$b = 180 - 2\phi_i = 159.1774^\circ$$

$$c = 180 - a - b = 0.0113^\circ$$

$$A = \frac{B \cdot \sin a}{\sin b} = 99948.141 \text{ m}$$

$$C = \frac{B \cdot \sin c}{\sin b} = 55.481 \text{ m}$$

$$D = A + C = 100003.622 \text{ m}$$

$$\tau_L = \frac{D - B}{\text{Speed of light}} = \frac{100003.622 \text{ m} - 100000.0 \text{ m}}{299792458 \frac{\text{m}}{\text{sec}}} = 12.081 \text{ nsec} \quad (1)$$

The scenario above would likely occur in a rural environment where the primary source of multipath is the reflection off the ground. In the second scenario, we look at a more urban

[illegible]

Similar calculations can be completed to find reflected path (denoted as A + D):

We have a range to select the multipath tolerance: $12 \text{ nsec} < T_g < 143.4 \text{ nsec}$. We double the range to add margin: $24 \text{ nsec} < T_g < 287 \text{ nsec}$. We initially set the Cyclic Prefix ratio to useful data symbol duration at $\frac{1}{8}$. We constrain the number of OFDM symbols per frame as an integer value, the system sampling frequency range $3.125 \text{ GHz} < F_s < 5.0 \text{ GHz}$, number of data subcarriers (SU) = 782 (see digital portion for derivation) and desire clock frequencies rounded to the nearest MHz for ease of setting the system oscillators. Through iterative calculation of the system parameters, we chose $T_g = 55.556 \text{ nsec}$. We can derive the rest of the OFDM parameters as follows:

$$\begin{aligned}
T_g &= 55.556 \text{ nsec}, SU = 784 \\
T_b &= 8 \cdot T_g = 444.444 \text{ nsec} \\
T_s &= T_b + T_g = 500 \text{ nsec} \\
\Delta f &= \frac{1}{T_b} = 2.25 \text{ MHz} \\
R_s &= \frac{1}{T_s} = 2 \text{ MBaud} \\
\text{Occupied BW} &= SU \cdot \Delta f = 1.764 \text{ GHz} \\
F_s &= \frac{N}{T_b} = 4.608 \text{ GHz}
\end{aligned}$$

These parameters are the basis for the rest of the system definitions.

Forward Error Correction

Several FEC techniques were investigated to ensure the transmitted information survived corruption due to analog component nonlinearities, channel affects, multipath, asynchronous sampling at receiver, among others. The requirement of peak data rate of 25 Gbps requires fast, deterministic and parallelizable FEC. Four categories of FEC were examined, namely: single Reed-Solomon (RS) or Bose-Chaudhuri-Hocquenghem (BCH) codes, low-density parity-check (LDPC) codes, inner-outer combination codes, and continuously interleaved (CI) inner-outer codes. These are described with positive and negative traits in Table 1 below.

Table 1: Comparison of Forward Error Correcting Techniques

FEC Scheme	Description	Notes
(1) Long RS or BCH	Single code for error correcting	Poor burst correcting capability
LDPC Codes	Large sparse coding matrices	a) Requires large matrices in memory b) Coding gains require iterative decoding
Inner-Outer	FEC on data, then FEC on FEC	Good burst correcting capability
CI Inner-Outer	Interleaver between inner and outer code	a) Improves burst error correcting over non-CI b) Reduces PAPR

The Continuously-Interleaved inner-outer codes have a good trade-off between complexity and error correcting performance. In addition, it reduces the PAPR of the OFDM symbol by the interleaver. The block diagram of the FEC is found in Figure 5.

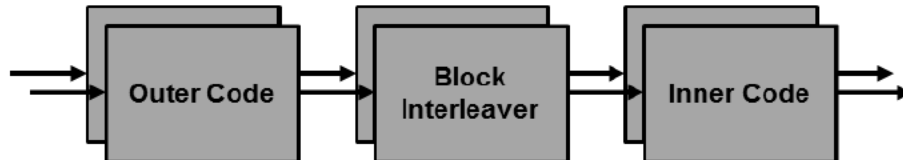


Figure 5: Forward Error Correction block diagram

The exact choice of (n,k) block codes depend on the OFDM symbol subcarrier count, while fitting all FEC code words within a single OFDM symbol. Since 16-QAM is the default

modulation scheme on each subcarrier, the number of message bits per FEC symbol is 3136. A few schemes were selected with overhead of 6%, 8%, and 10% for CI-BCH and CI-RS, as well as, the RAPIDLink inner-outer code [RS(255,239); BCH(127,120)] and the 802.16 (WiMax) specification. The plot in Figure 7 showcases the bit error rate versus channel SNR over an AWGN channel for the various FEC schemes. The objective operating bit error rate is $1e-8$, at the bottom of the y-axis where it meets the x-axis. Although CI-BCH 10% performs slightly better (results in slightly higher net coding gain) than the CI-RS schemes, the overhead wasted in comparison to CI-RS 8% is negligible.

Peak to Average Power Ratio

The PAPR is a major concern with the implementation of OFDM. Unlike single carrier systems, the time domain envelope has large variations due to multiple data symbols constructively and de-constructively interfering in phase. This affects the received data symbols on all subcarriers of an OFDM symbol (inter-symbol interference) and affects out-of-band emissions, increasing adjacent subcarrier interference (inter-carrier interference).

To combat the large operating range, power amplifiers are forced to operate within the linear region (usually limited and at a lower power) to prevent carrier distortion. This may also force DAC input levels to be backed off, lowering the effective number of bits (ENOB) it provides. Furthermore, a scarcity of HPAs (High Power Amplifiers) at the system's RF frequencies (71-76 GHz and 81-86 GHz), encourages PAPR reduction due to cost and selection. A pictorial representation of PAPR is given in Figure 6.

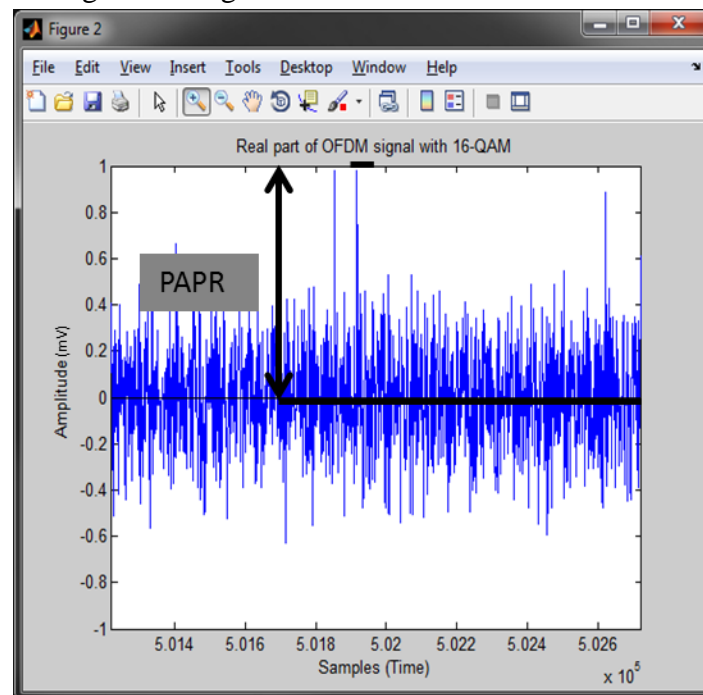


Figure 6: Time domain of OFDM demonstrating high PAPR

Several PAPR reduction techniques were investigated, including those that fall with categories of block coding, selective mapping, clipping/filtering, tone reservation, and companding.

Ultimately, two techniques were selected for their simplicity, namely: Clipping/Filtering and Error Function Companding. First, Clipping/Filtering limits the magnitude of the signal to a threshold ξ and filters to reduce out of band interference caused by injecting higher frequency transitions in the original signal. Typically, the Kaiser filter is utilized in this regard. Figure 7 demonstrates the purpose of the Clipping/Filtering process.

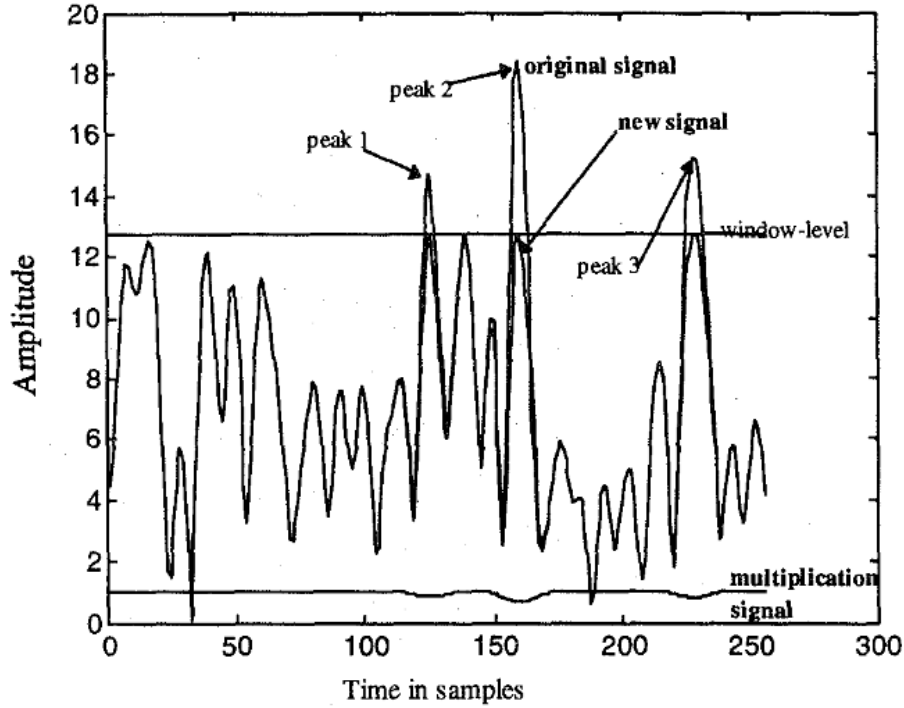


Figure 7: Clipping/Filtering process

Secondly, a more computationally intense scheme is selected that yields more PAPR reduction. The purpose of companding is to transform OFDM signals that are distributed exponentially into uniformly distributed signals through a lossless (invertible) transform. Companding enlarges small samples while reduces large ones, yet maintains the original average power. The companding technique requires calculating the error function of the input, hence its name. The transmitter transforms the desired OFDM symbol by:

$$h(s_n) = k_1 \cdot \text{erf}(k_2 \cdot s_n) \quad (3)$$

where s_n is the input OFDM symbol sample, k_1 and k_2 are predetermined scalars and

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt.$$

At the receiver, each transformed symbol sample is returned to the desired OFDM symbol sample by:

$$s_n' = \frac{\text{erf}^{-1}\left(\frac{h(s_n)}{k_1}\right)}{k_2}. \quad (4)$$

Equalization

Equalization in OFDM systems typically consists of multiplication of each subcarrier with a scalar value to attain the desired amplitude. Since the operating band (approximately 2 GHz) is divided into $N = 2048$ subcarriers, the spacing is approximately 1 MHz. Similarly to integration of continuous functions, we can assume the frequency response is relatively flat for each subcarrier. For example, if our response was the red line in Figure 8, subcarriers $x < 1.0$ would be multiplied by larger scalars than $x > 1.0$ to attain a uniform response $y = 1.0$. The equalization would be determined from the analog transmitter components to counteract their nonlinear affects.

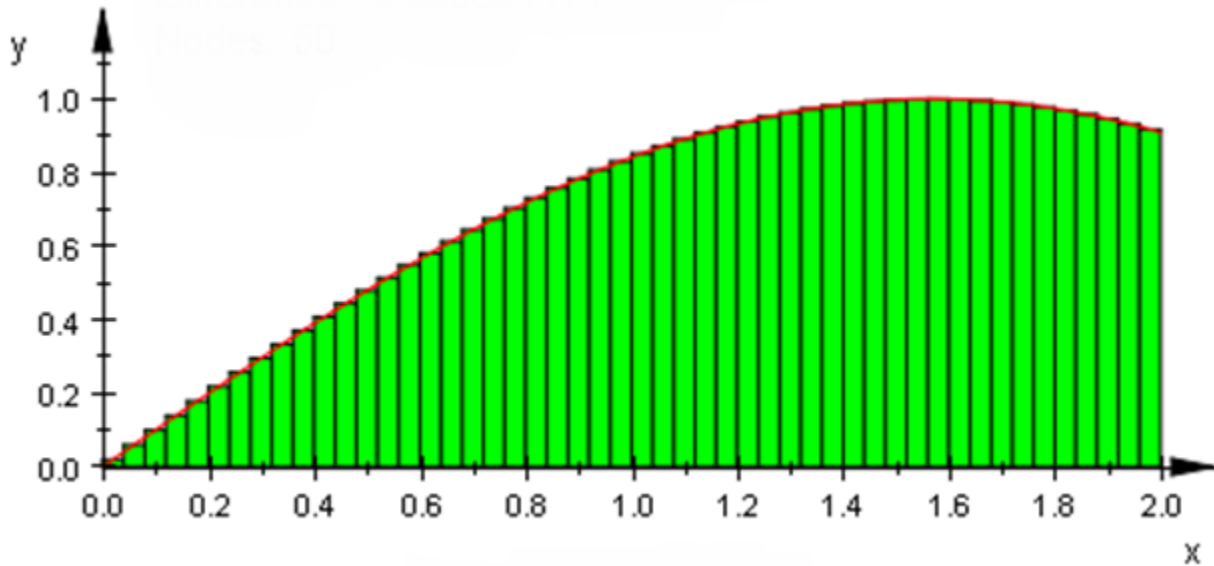


Figure 8: Example of approximating continuous function with scalar (flat) values

Synchronization

The digital synchronization of the system has two phases, one for time synchronization and the other for frequency synchronization. Both utilize known pilot pseudo-random noise sequences transmitted on several subcarriers dispersed through the operating band. Multiple pilot carriers ensure frequency dependent effects do not affect the entire OFDM symbol. The technique selected was originally purposed by Minn, which utilizes complex conjugate pair sequences to reduce false positives when correlating and determining the start of the symbol. For a pilot sequence of length K , the sequence is constructed as:

$$B = [A \bar{A} A \bar{A}]$$

where A is a $\frac{K}{4}$ pseudo-noise sequence and \bar{A} is the complex conjugate of A . For time synchronization, the measurement of the correlation is calculated by:

$$M(d) = \frac{|P(d)|^2}{R(d)^2}$$

$$P(d) = \sum_{m=0}^{\frac{N}{2}-1} \bar{r}(d-m) \cdot r(d+m) \quad (5)$$

$$R(d) = \sum_{m=0}^{\frac{N}{2}-1} |r(d+m)|^2$$

where r is received signal, d is current index in r , and m is offset index. The maximum indicates alignment and the intended sampling time. For frequency synchronization, the adjustment in frequency can be found for each carrier by:

$$\Delta f = \frac{\text{angle}(P(d))}{\pi T}. \quad (6)$$

Model and Simulation of Flexible Data Link System Characteristics

All simulations for the physical layer components described in this report were simulated within MATLAB[®]. In the following sections, we split the simulations to isolate the operation of each major block to demonstrate the utility for our operating requirements.

Digital Upconversion / Digital Downconversion

The use of digital upconversion and digital downconversion greatly reduces the physical footprint of the analog components. The simulation below involved generating RAPIDLink symbols (QPSK) that is oversampled by 2 and pulse shaped by a root raised cosine filter. The digital conversion is completed by oversampling the data by 2 (for a total oversample of 4) and multiply the in-phase channel by a cosine wave and the quadrature channel by a sine wave at the up-sampled frequency.

In Figure 9, the baseband QPSK waveform is shown (in-phase channel only). This would be the nominal spectrum of the transmitted data before upconversion (whether via analog components as is performed in the RAPIDLink system or within the FPGA and DAC as in the Flexible Data Link system). This signal is digitally upconverted to an intermediate frequency (IF) centered around 1.412 GHz and shown in Figure 10. This signal would be further upconverted to Ka band (for RAPIDLink operation) or E band (for Flexible Data Link operation). Figure 11 showcases the received signal (in blue) digitally downconverted and the desired symbols (in red).

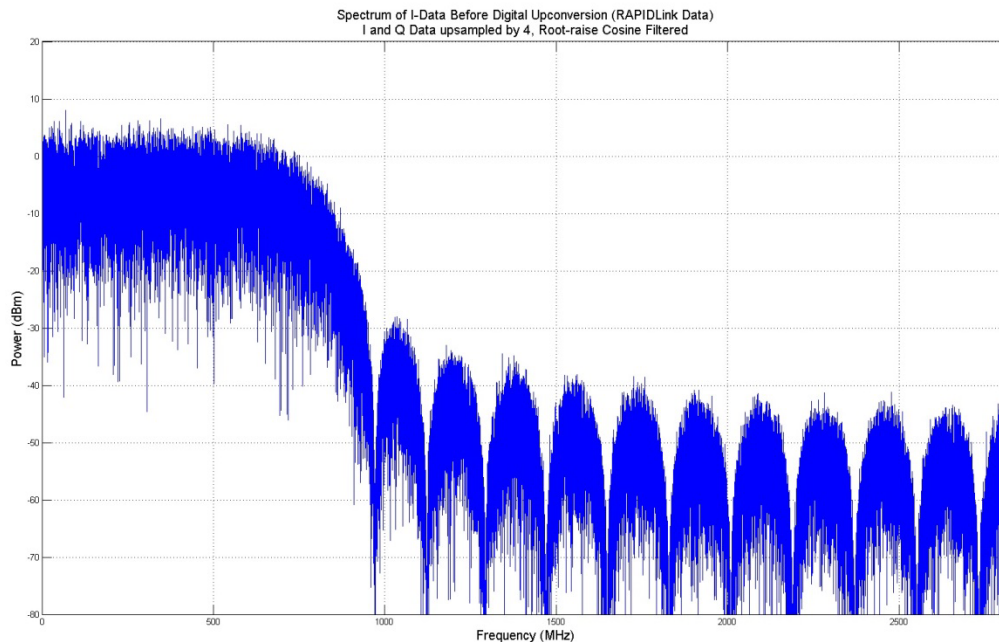


Figure 9: Baseband spectrum of in-phase channel (before digital upconversion)

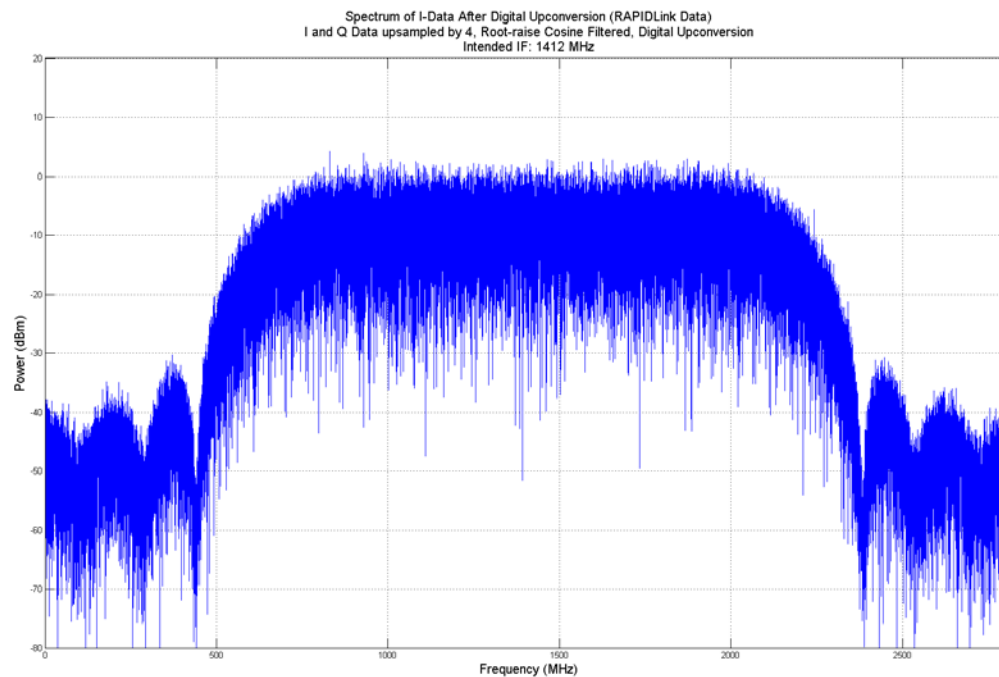


Figure 10: Intermediate frequency spectrum of in-phase channel (after digital upconversion)

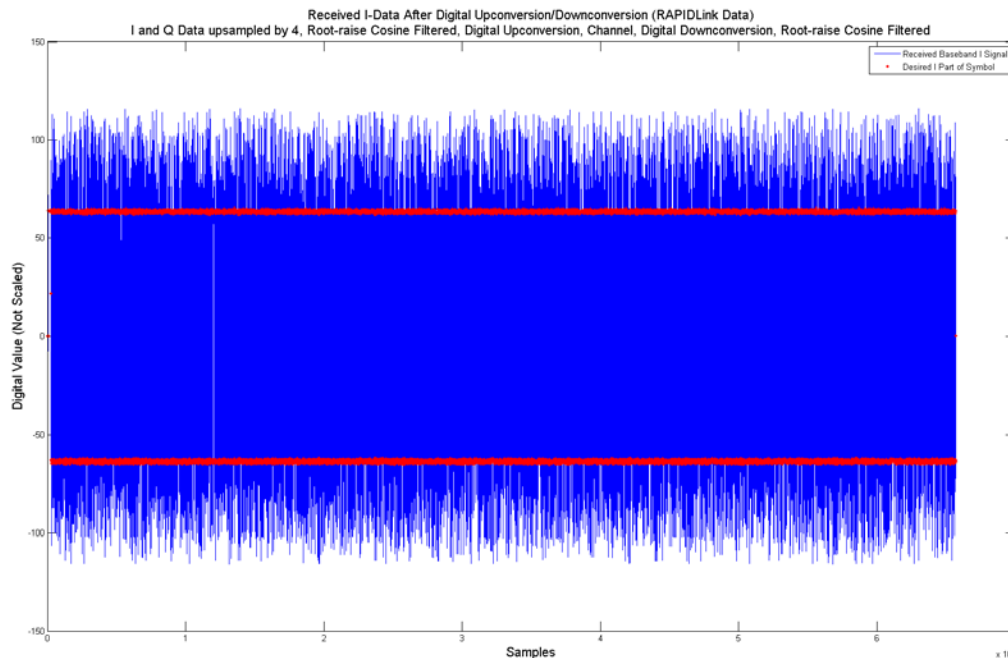


Figure 11: Time domain signal and symbols of in-phase channel (after digital downconversion)

Forward Error Correction

As described in the previous section, the forward error correction scheme selected will greatly assist in achieving the desired distance, data rate and reliability requirements of the Flexible Data Link system. The bit error rate curves shown in Figure 12 were found by encoding 16-QAM symbols and receiving and decoding after an AWGN channel with SNR at 0.5 dB increments. The ideal (un-coded) 16-QAM bit error rate is in black with schemes including the current RAPIDLink inner-outer code [RS(255,239); BCH(127,120)], the 802.16 (WiMax) specification and various continuously-interleaved inner-outer schemes.

A Monte Carlo simulation was performed for each scheme at each channel SNR until a minimum of 100 received bit errors were realized (when compared to the desired bit values). Three schemes performed similarly for a receiver bit error rate of $1\text{E-}8$. Of these three, the continuously-interleaved Reed-Solomon scheme with 8% overhead has the best trade-off of performance (net coding gain) and overhead. Therefore, this is selected as the default for the Flexible Data Link system.

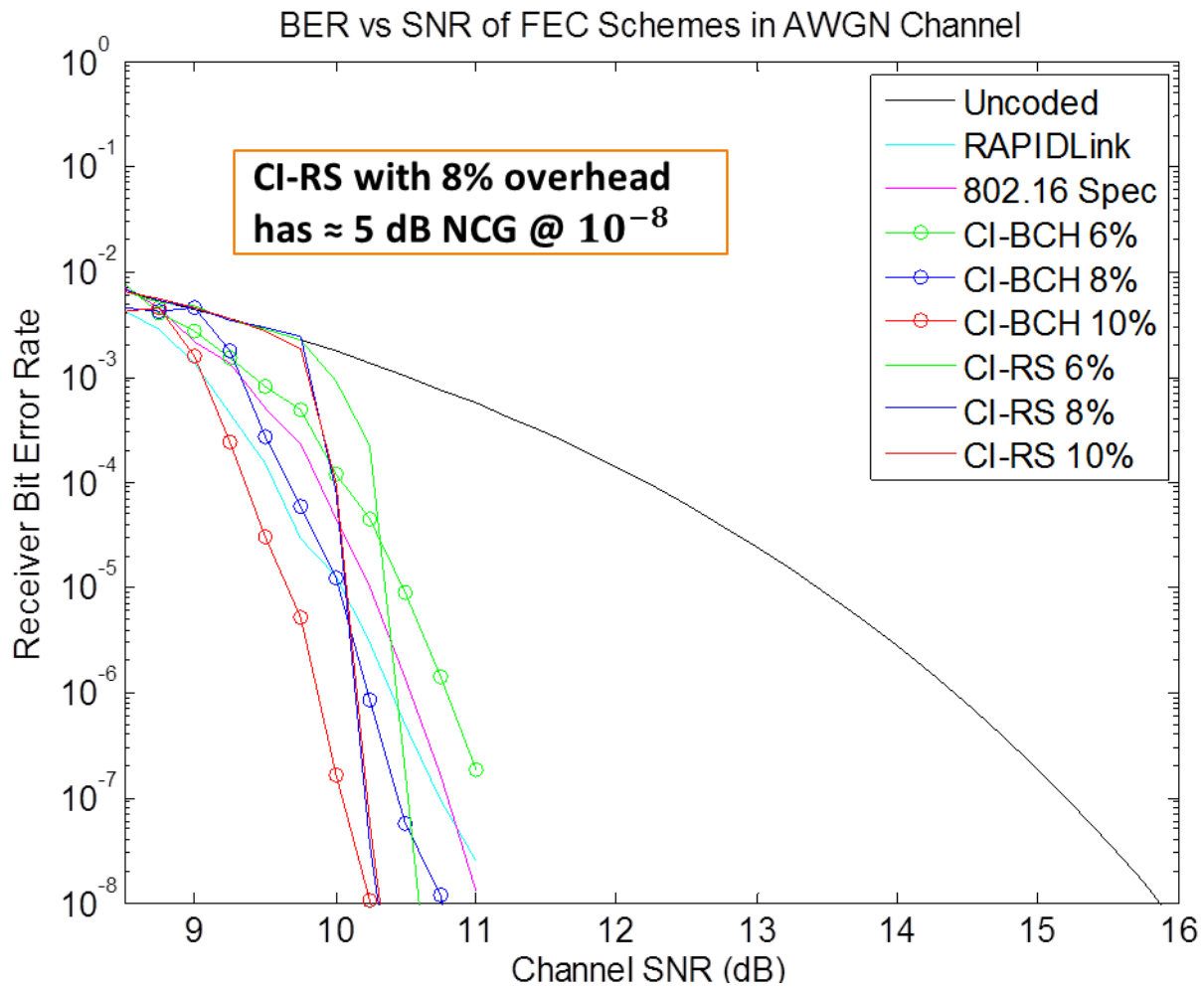


Figure 12: Bit error rate comparison of FEC schemes

OFDM

The default modulation technique in the Flexible Data Link system is 16-QAM on top of Orthogonal Frequency Division Multiplexing. This can be adjusted on one or more (or all) carriers to ensure delivery of the data. The spectrum of the digitally upconverted OFDM signal is found in Figure 13. This has modulated 16-QAM data on each carrier with the overall bandwidth of 1.94625 GHz with guard carriers turned off on each side of the intended data.

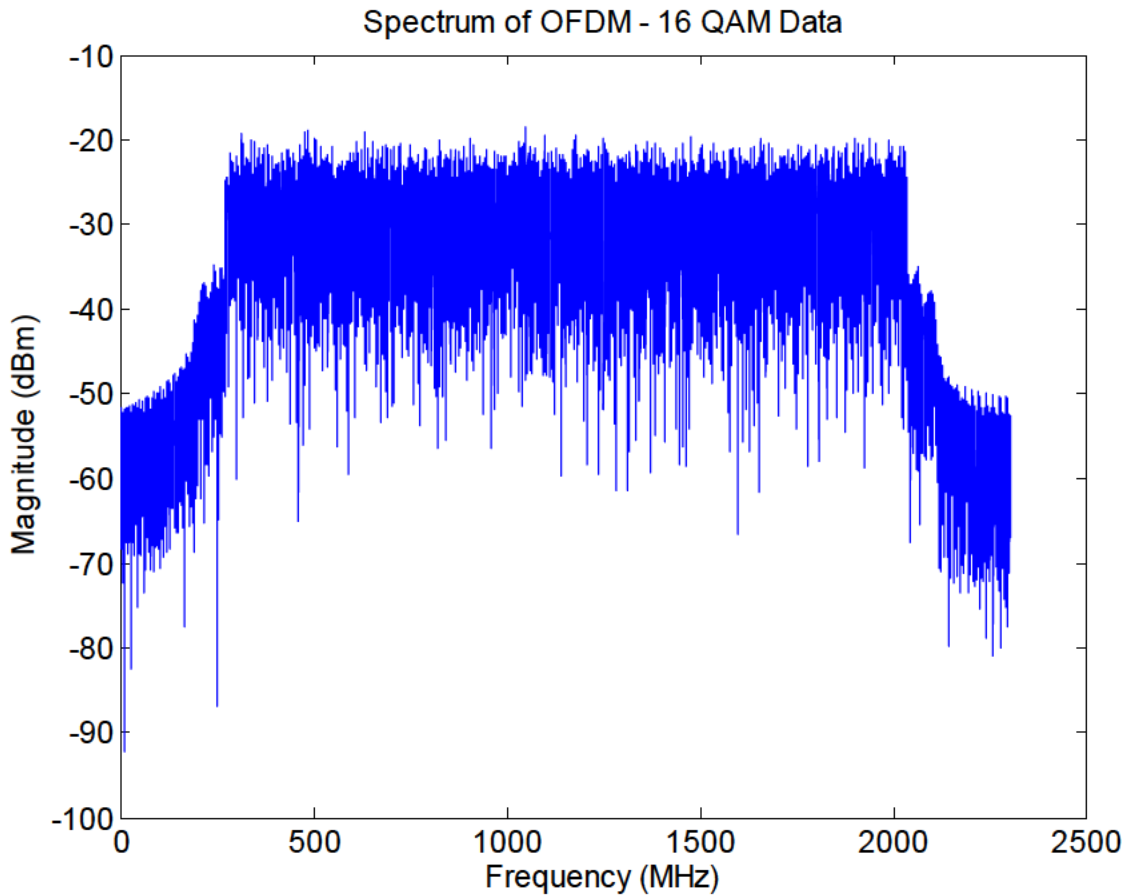


Figure 13: Spectrum of 16-QAM data on OFDM carriers digitally upconverted

Peak to Average Power Ratio Reduction

The peak to average power ratio reduction techniques introduced in the previous section processed the OFDM signal after the IFFT (in the time domain). In Figure 14, the dotted blue line represents the original signal with samples above the orange boundaries that signify the operating range of the DAC. The PAPR reduction techniques (clipping in black, error function in green and exponential in red) show significant reduction in the samples that fall outside this range. The exponential companding technique requires continuous parameter updating that must be passed between the transmitter and receiver that makes it operationally infeasible. The other two techniques are adequate to operate within the Flexible Data Link system, with clipping being the first choice and error function companding being the second.

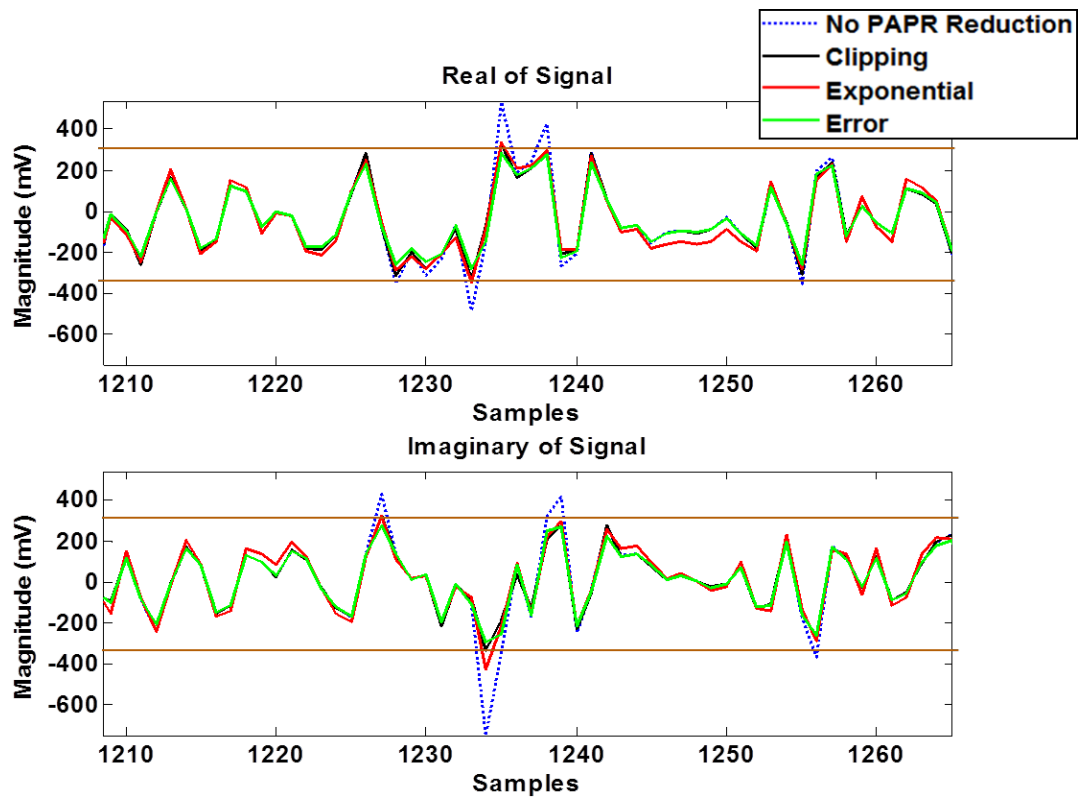


Figure 14: Time domain of OFDM symbol with various PAPR reduction techniques

Flexible Data Link Digital Design

As previously mentioned, the Flexible Data Link system has been designed for a peak data-rate performance of 25 Gbps. Because of limitations in existing DAC and ADC technologies, the digital transceiver has been designed as a multiplexing of four independent DACs and ADCs, each independently capable of 6.25 Gbps. To maintain a modular design approach, the digital boards have been envisioned such that two DAC and two ADC channels will be available per each Open VPX, 6U card. A block diagram of this design is shown in Figure 15.

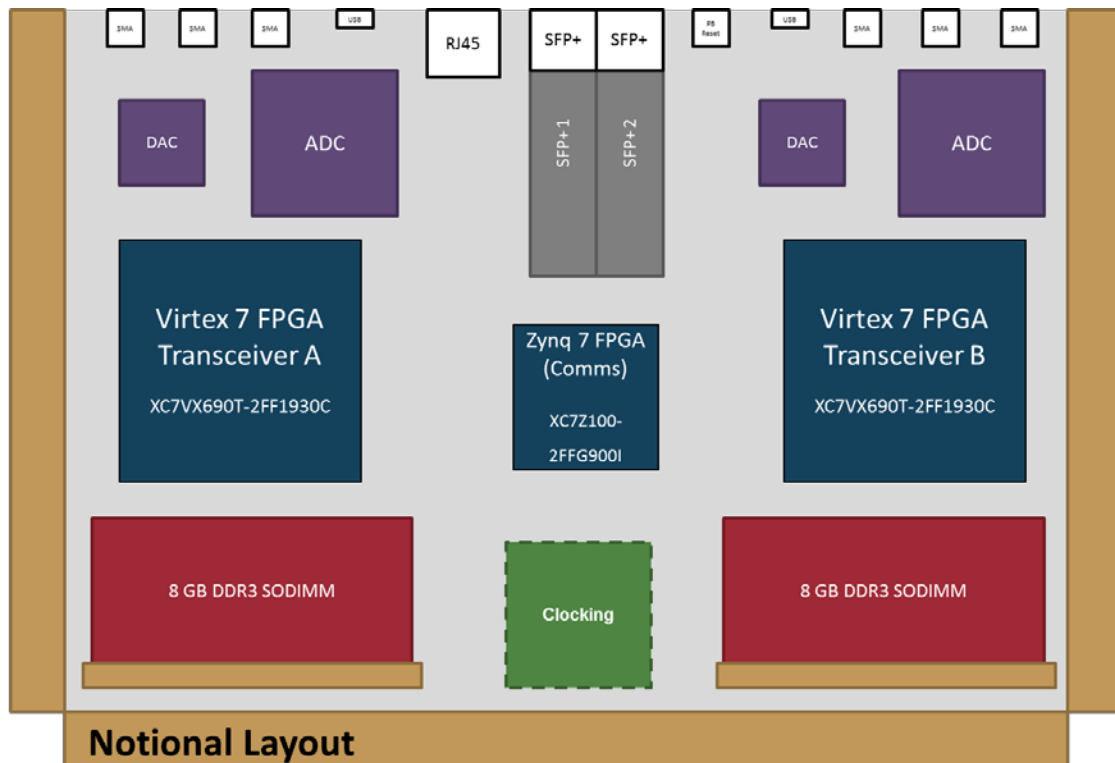


Figure 15: Notional Digital Board Layout

Each Virtex 7 FPGA shown in Figure 15 are independent transceivers, capable of a single channel transmit and receive capability at the 6.25 Gbps data-rate. SMA connectors on the front of the board will allow interfacing with the DACs and ADCs, while SFP+ connections will allow for high-speed IP-based interfacing with the board, managed by the Zynq FPGA. DDR3 SODIMMs will allow for direction injection of waveforms, providing a capability similar to an arbitrary waveform generator, important for testing. A more detailed view of these interfaces is shown in Figure 16.

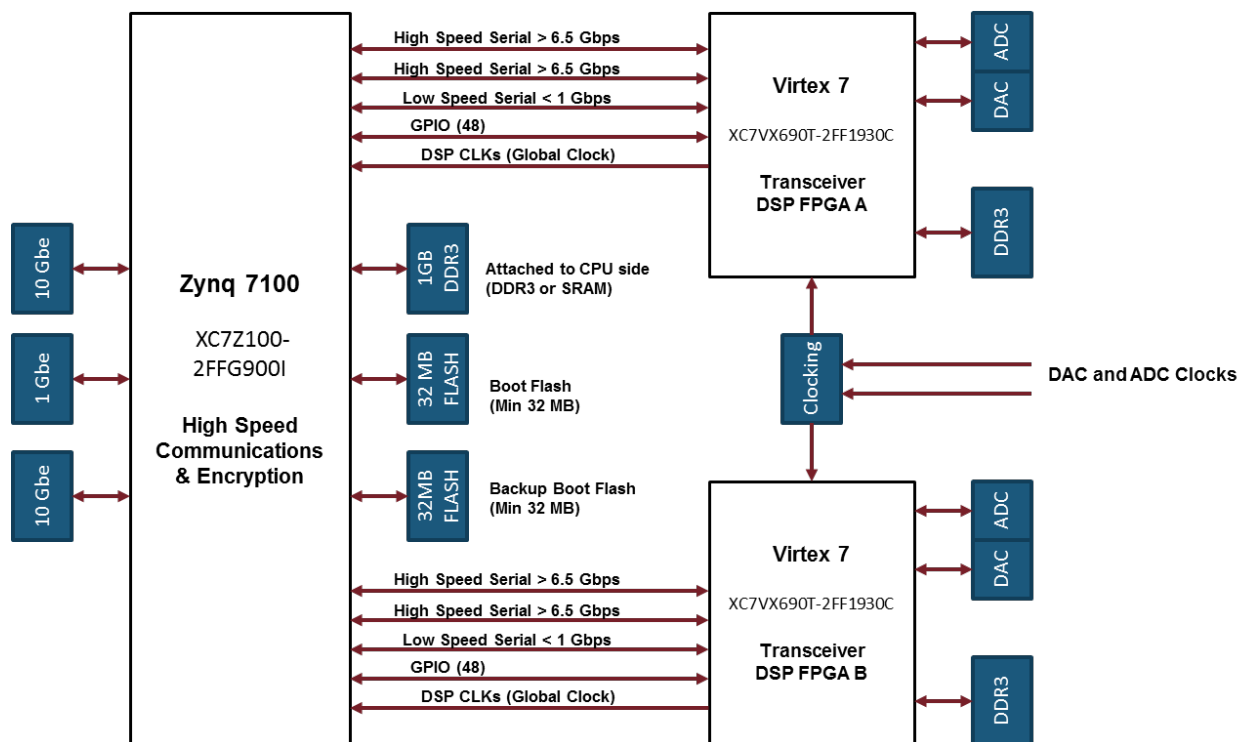


Figure 16: Digital Board Block-level Design

FPGA Design

Digging deeper into each of the FPGAs, the design for each of the Virtex 7 transceiver FPGAs is identical to support modularity and flexibility of adding or removing additional transceiver cards. A conceptual flow diagram of this FPGA image is shown in Figure 17.

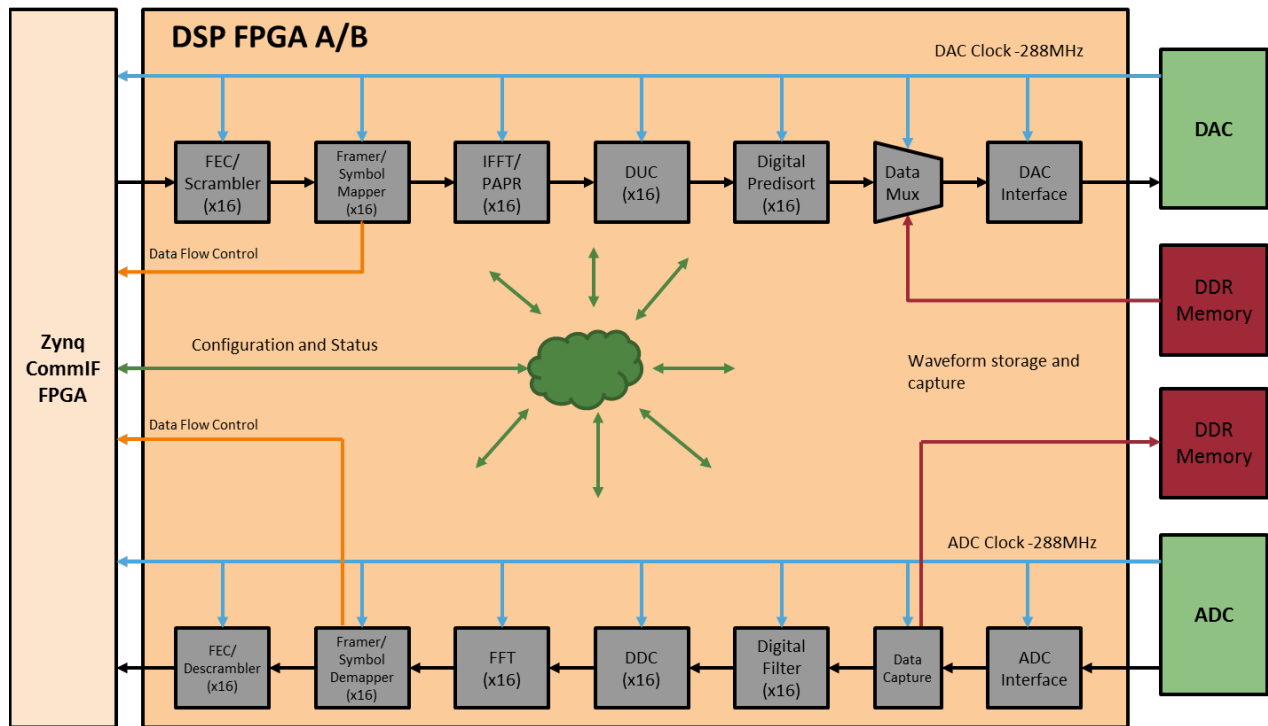


Figure 17: Transceiver DSP FPGA

As mentioned in previous sections, the design of the Flexible Data Link system is such that it can be easily adapted to support changing communications operations (waveform, FEC, power, etc) as well as the flexibility to support entirely different operational modes (communications, sensing, RADAR, etc).

Figure 17 shows the basic structure as related to the communications chain for an OFDM waveform. In the Flexible Data Link system, each of the communications blocks will be strongly typed and stored as available communication engine blocks within the FPGA. If the mode of operation changes such that different operational blocks are required, those can be swapped in and enabled on-the-fly.

An example of this process is the IFFT/FFT processing blocks. In an OFDM communications waveform, the IFFT and FFT blocks are necessary to convert data to and from the time domain. However, the FFT block is also useful for spectrum sensing, where an FFT block can provide a snapshot of the current operating radio frequency spectrum, allowing for everything from dynamic spectrum access techniques to waveform notching and directional nulling technologies. By making each of the available communications blocks available in this way, these operational changes can be made rapidly.

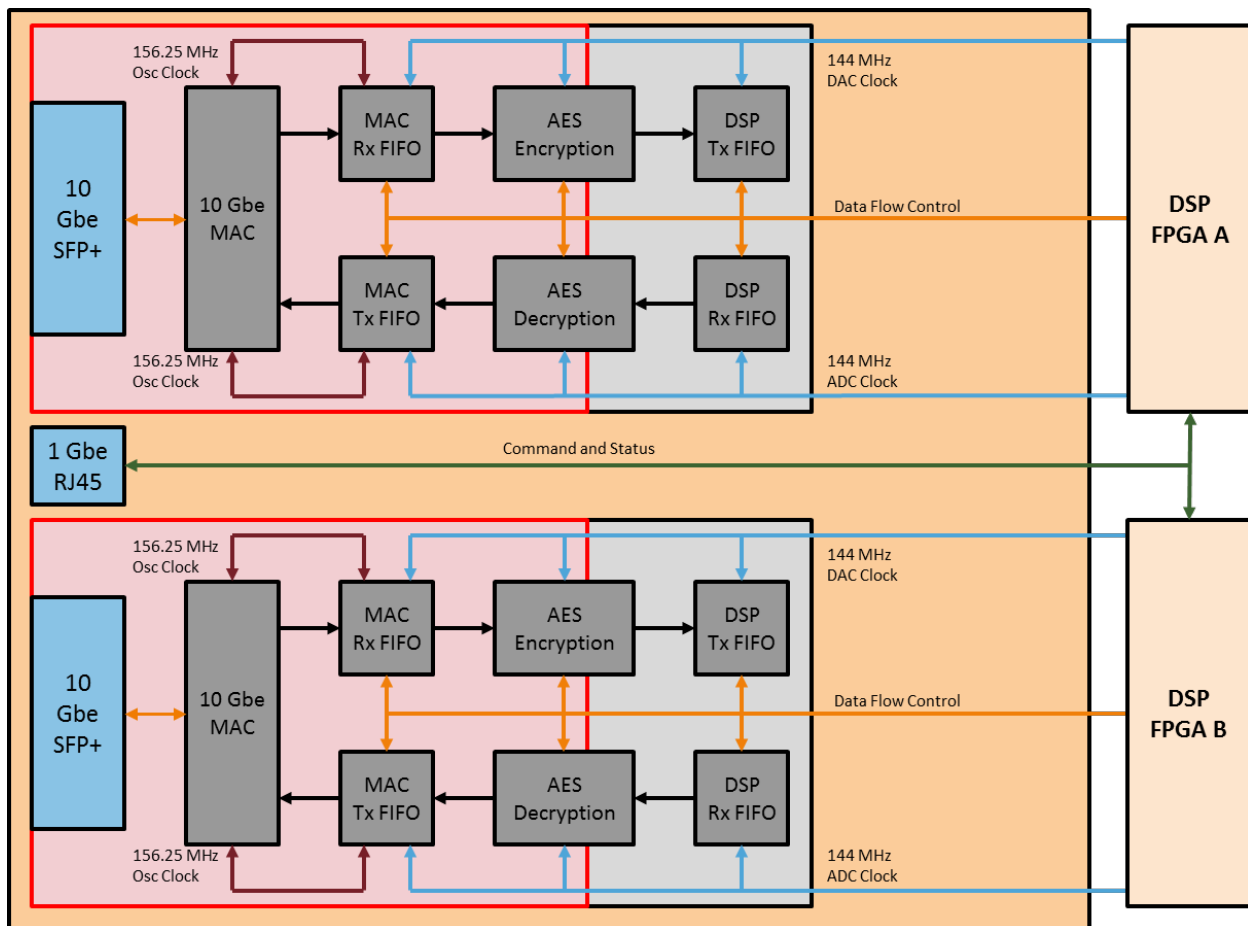


Figure 18: High Speed Communications and Encryption FPGA

The final FPGA located on the digital card is the Zynq FPGA, used for high speed communications and encryption. Shown in Figure 18, this FPGA takes 10 Gbe packets from the SFP+ modules and routes them through the onboard MAC and encryption blocks and out to the Transceiver DSP FGAs. Since these are full transceivers, this process happens in both transmit and receive directions for each DSP FPGA. Since each of the SFP+ interfaces as well as the DSP FPGA interfaces are independent of one another, the operations within the communications and encryption FPGA are duplicated for each transceiver channel.

DAC and ADC Interface

To interface with the analog domain, the DACs and ADCs must be interleaved to support the data rates and bandwidths desired. On the transmit side, the DAC will interleave 16 independent channels at 288 MHz each, for a total of 4.608 GSPS. This multiplexing is done in two blocks as shown in Figure 19. First, 12 bits of each of the 16 channels are passed through four 4:1 DDR OSerdes, creating four lanes at 1.152 GSPS. Then each of these 4x12 bit lanes is passed into the DAC, culminating in the final 4.608 GSPS.

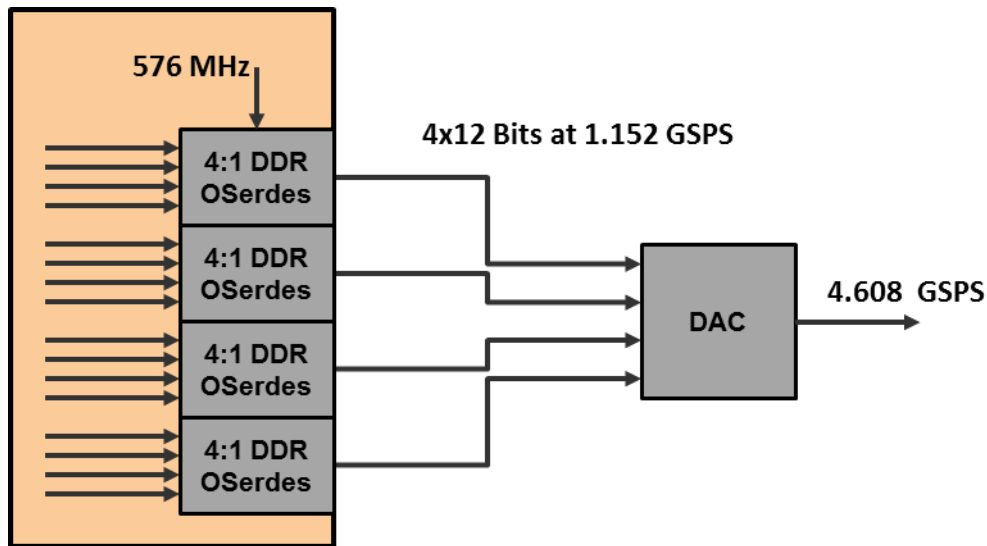


Figure 19: DAC Multiplexing

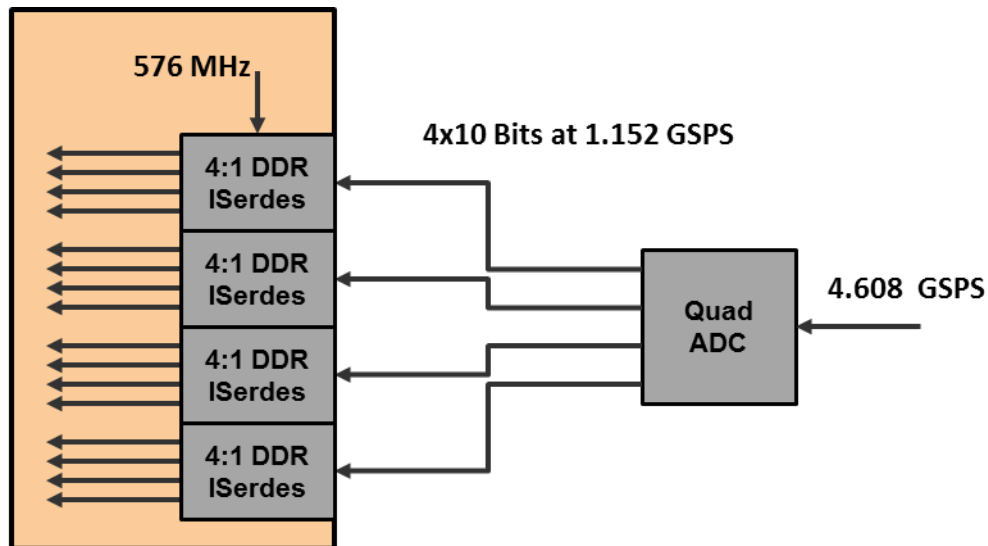


Figure 20: ADC Multiplexing

The process is nearly identical on the receive side as shown in Figure 20, where the signal is passed into the ADC chip at 4.608 GSPS and is demultiplexed into the original 16 channels at 288 MHz. Due to the capabilities of the proposed ADC, the received data will be 10 bits in length instead of the 12 bits per channel at the transmitter.

Flexible Data Link Analog Design

To obtain a maximum data rate of 25 Gbps, a tradeoff exists between the amount of spectrum required and the spectral efficiency of the proposed waveform in b/s/Hz. More spectrally efficient waveforms require less spectrum, but require a higher signal to noise ratio (SNR) that creates additional design challenges.

To remain flexible for changes in requirements as well as to reduce overall design risk, it was determined to assume a spectral efficiency of no more than 4 b/s/Hz. This is consistent with a waveform such as 16-QAM or 16-APSK. Higher spectral efficiencies may be possible, but to rely on higher order modulation techniques was an unnecessary challenge to the design.

Spectral Utilization

Assuming a maximum spectral efficiency of 4 b/s/Hz and a peak data rate of 25 Gbps, the minimum spectral utilization would be 6.25 GHz. Additionally, waveform processing and overhead such as peak to average power ratio mitigation, forward error correction, multipath mitigation, and packet and frame headers require additional bandwidth. Based on analysis and simulation, it was determined that 8 GHz of available spectrum was necessary to ensure proper operation.

Given the 8 GHz requirement and the limitations of Shannon sampling and the desire for digital upconversion, the requirements on a DAC would have been greater than 16 GSPS. As discussed in the digital design section, we instead chose to break the system (and thus operating spectrum) into four independent sections, each with approximately 2 GHz of spectral bandwidth. This greatly reduces the requirement on the DAC and ADC.

Even so, the requirement for total available spectrum of at least 8 GHz still existed. From this requirement, the determination was made to take advantage of available spectrum in the 71-86 GHz bands (E-band, also known as V&W bands). Specifically, the spectrum usage was designed to support two independent bands from 71-76 GHz and second set from 81-86 GHz. A graphic of the spectral utilization is shown in Figure 21.

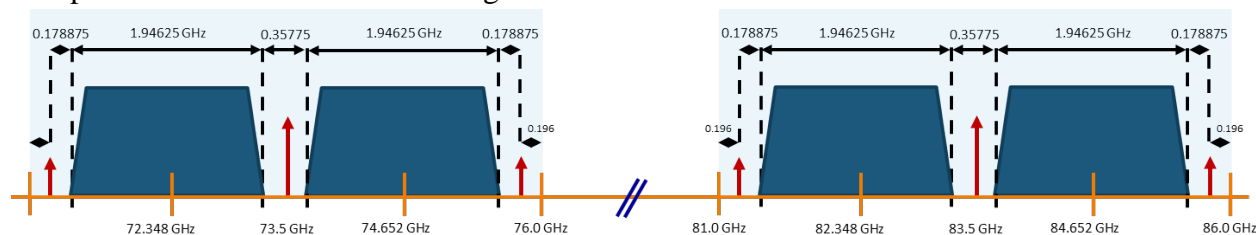


Figure 21: Occupied Spectrum at E-band

Note that a buffer of over 350 MHz exists between each of the transceiver pairs. This is necessary to provide room for analog filtering at the lower frequencies, as well as provide room for rolloff of each of the waveforms. Additional buffers exist on either side of the waveforms to eliminate the potential for out-of-band signaling.

Intermediate Frequency Upconversion

To achieve the analog multiplexing of waveforms as well as the upconversion to E-band, a multi-stage upconversion scheme was developed. The block diagram of the first upconversion stage is shown in Figure 22.

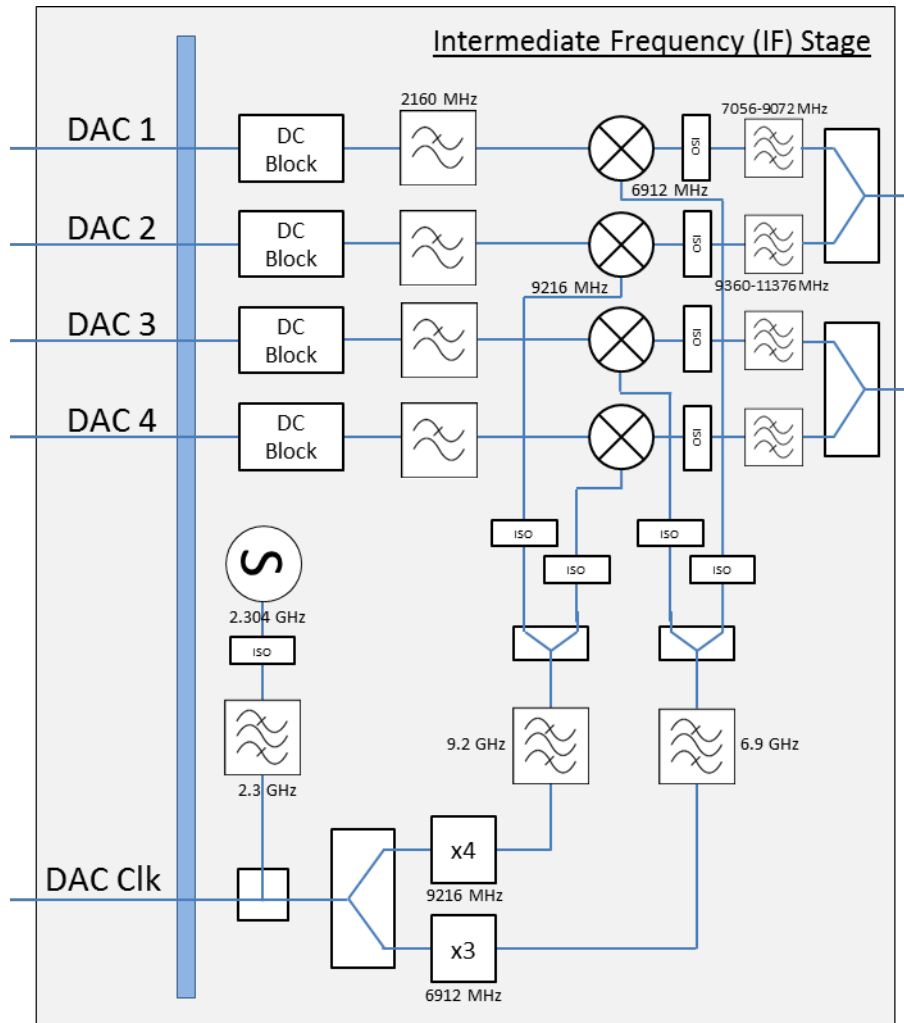


Figure 22: Intermediate Frequency Upconversion Stage

In Figure 22, the four independent transceivers (each fronted by a DAC) are low-pass filtered and mixed up to an intermediate frequency. Two of the channels are mixed up with a 6.912 GHz local oscillator, while the remaining two are mixed with a 9.216 GHz oscillator. This signal is generated from a single 2.304 GHz source, which also drives the clocks for each of the DACs. Once upconverted to their IFs, each pair of signals can be combined onto the same analog channel, utilizing the spectrum from 7056-9072 MHz. While shown as a set of filters and combiners, a diplexer operating in these bands would provide reduced channel loss. Once at the identified IF, each of the two output channels can be independently upconverted to the 71-76 GHz and 81-86 GHz bands and amplified for transmission over the air.

Atmospheric Absorption

The RF Link Budget drives the transmission distance of the proposed Flexible Data Link system, as well as provides requirements on power amplifiers and receiver noise that are otherwise unavailable. Since the intention is to operate the system at E-band, it is first necessary to determine atmospheric absorption as a function of water vapor and oxygen, in addition to free

space path loss. The chart in Figure 23 identifies these losses in dB/km, and their approximate impact at our bands of interest.

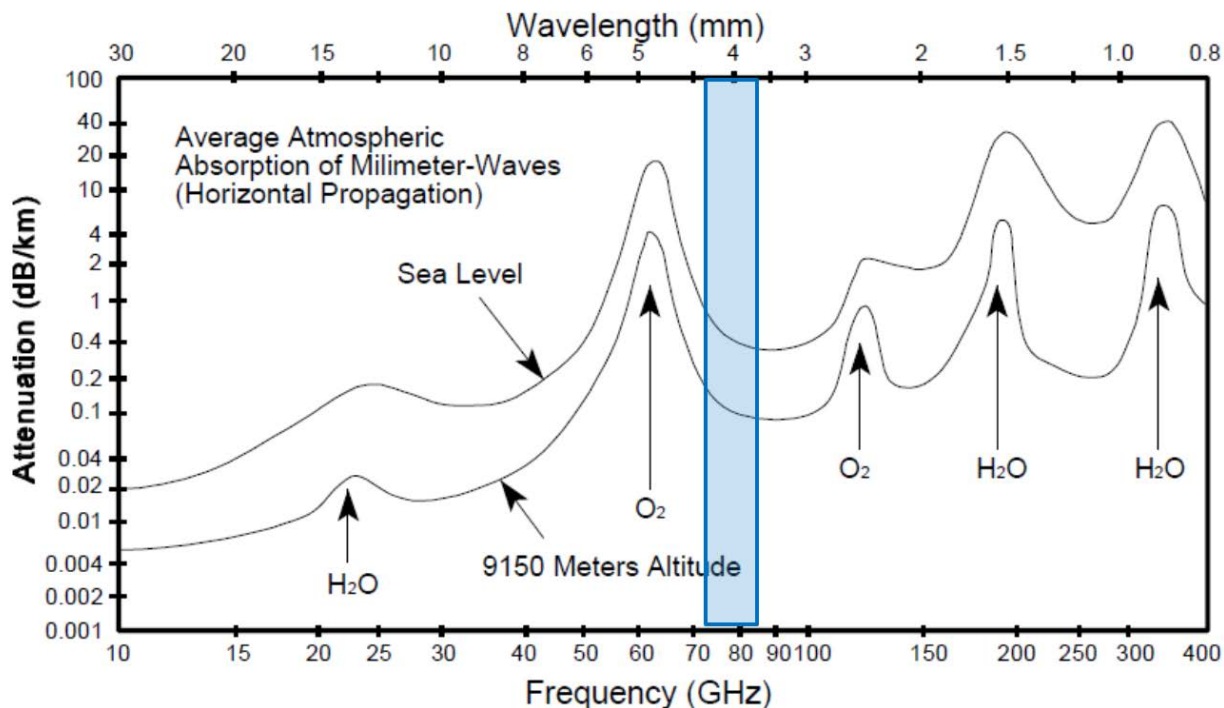


Figure 23: Oxygen and Water Absorption as a Function of Frequency

As shown, the E-band frequencies are of interest to us as they exist just beyond the spike in atmospheric absorption near 60 GHz. Additionally, the Figure shows the significant disparity between attenuation at sea level versus at a 9150 meter altitude. As the Flexible Data Link system is an airborne asset which may operate above the 9150 meter line shown, a safe attenuation factor of 0.1 dB/km is assumed.

Link Budget

Next the actual link budget equations are considered, to determine requirements on antenna reflector and power amplifier size. Given our known bit rate and operating frequencies, the equation described in Figure 24 can be iterated upon. Assuming a peak transmission distance of 100 km and a 16-QAM waveform (which requires 16 dB SNR at the digital receiver), 10 dB of link margin for atmospheric absorption, 4.5 dB of transmit back-off for peak to average power ratio mitigation, 4.5 dB of FEC coding gain, and 24 inch Cassegrain reflectors, we arrive at a required transmission power of 32.7 dBm.

As with any system such as this, tradeoffs exist which can be adjusted to increase or reduce loss in a given area. For instance, an airborne reflector might be limited to 10 or 12 inches in diameter, necessitating higher coding gain at the FEC, higher transmission power, etc.

- $\frac{E_b}{N_0} (SNR) = \frac{C}{N_0} - 10 * \log R_b$
 - E_b = Signal power
 - N_0 = Noise power
 - C = Carrier power
 - R_b = Bit rate (b/s)
- **Carrier to noise ratio can be further reduced:**
 - $\frac{C}{N_0} (dB - Hz) = PEIRP - L + \frac{G}{T_{sys}} + K$
 - P_{EIRP} = Equivalent Isotropically Radiated Power (dBW)
 - L = Theoretical path loss (dB)
 - G = Receive gain (dB)
 - T_{sys} = System temperature (K)
 - K = Boltzmann's Constant = 228.7 (dB-Hz)
 - Each of these factors can be further broken down:
 - $P_{EIRP} = P_t + G_t - L_t - 30$ (dBW)
 - P_t = Transmit power (dBW)
 - G_t = Transmit antenna gain (dBi)
 - L_t = Loss between transmitter and antenna (dB)
 - $L = 147.56 - 20\log(f) - 20\log(d)$ (dB)
 - f = Frequency (Hz)
 - d = Transmit distance (m)
 - $G/T_{sys} = G_r - 10*\log(N_{fr} + T_r)$
 - G_r = Receive antenna gain (dBi)
 - N_{fr} = Receiver noise factor = $(10^{N_{fig}/10} - 1) * T_g$
 - N_{fig} = Noise Figure (dB)
 - T_g = Ground Temperature = 290 (K)
 - T_r = Antenna perceived temperature = $(T_g + T_s) / 2 = (290K + 30K) / 2 = 160$ (K)
 - T_s = Sky temperature = 30 (K)
- **Final Link Budget Equation:**
 - $\frac{E_b}{N_0} = [P_t + G_t - L_t - 30] - [147.56 - 20\log(f) - 20\log(d)] + G_r - 10\log\{290 * (10^{N_{fig}/10} - 1) + 160\} + 228.7 - 10\log R_b$

Figure 24: Link Budget Equations for Target Environment

Conclusion

The Flexible Data Link system design comprises mathematical analysis, modeling and simulation, waveform design, analog and digital design, and system-level information brokering at every level of the OSI stack. The purpose is to change the game in radio frequency communications by creating a Government owned, flexible communications engine rather than a stove-pipe data link. The Flexible Data Link design is capable of supporting this, demonstrating that the next generation of communications systems is both realizable and achievable.

List of Acronyms:

ADC	Analog to Digital Converter
AFRL	Air Force Research Laboratory
APSK	Amplitude Phase Shift Key
AWGN	Additive White Gaussian Noise
BCH	Bose-Chaudhuri-Hocquenghem
CDR	Critical Design Review
CI	Continuously Interleaved
CP	Cyclic Prefix
DAC	Digital to Analog Converter
DDC	Digital Down Converter
DDR	Double Data Rate
DUC	Digital Up Converter
ENOB	Effective Number of Bits
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
Gbps	Giga bit per second
IF	Intermediate Frequency
IFFT	Inverse Fast Fourier Transform
LDPC	Low Density Parity Check
MAC	Medium Access Control
MHz	Mega Hertz
nsec	Nano seconds
OFDM	Orthogonal Frequency Division Multiplexing
OSI	Open System Interconnection
PAPR	Peak to Average Power Ratio
PDR	Preliminary Design Review
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Key
RF	Radio Frequency
RS	Reed-Solomon
S&E	Scientist & Engineers
SFP	Small Form-factor Pluggable
SIGINT	Signal Intelligence
SNR	Signal to Noise Ratio
SODIMM	Small Outline Dual In-line Memory Module
SU	Sub-carrier